We Claim:

1. A circuit configuration, comprising:

a programmable link for permanent storage of a datum;

a drive circuit containing:

a data input;

a complementary data input;

a drive circuit output coupled to said programmable link and outputting an energy pulse for activating said programmable link in a manner dependent on a data signal present at said data input;

a first transistor having a control terminal connected to said data input;

a second transistor having a control terminal connected to said complementary data input; and

a volatile memory for storing a datum, said volatile memory containing:

an output outputting the data signal being a memory content of said volatile memory, said output connected to said data input of said drive circuit for data communication, said control terminal of said first transistor receiving the data signal; and

a complementary output outputting a complementary data signal being complementary to the data signal and connected to said complementary data input of said drive circuit, said control terminal of said second transistor receiving the complementary data signal.

2. The circuit configuration according to claim 1, wherein said output of said volatile memory is directly connected to said data input of said drive circuit.

3. The circuit configuration according to claim 1, wherein said volatile memory has a memory cell.

4. The circuit configuration according to claim 3, wherein said memory cell has two inverters which are coupled with negative feedback to form a self-latching circuit.

5. The circuit configuration according to claim 1, wherein said drive circuit has an activation input for receiving an activation signal.

6. The circuit configuration according to claim 5, wherein said drive circuit has an AND logic circuit, said data input and said activation input being inputs for said AND logic circuit for performing an AND combination of the data signal and the activation signal.

7. The circuit configuration according to claim 1, wherein said complementary data input is directly connected to said complementary output of volatile memory.

8. The circuit configuration according to claim 1, wherein said drive circuit contains a blowing transistor having an input side coupled to said data input, a terminal for receiving a blowing voltage and, an output side coupled to said programmable link for transmitting a voltage pulse.

9. The circuit configuration according to claim 8, wherein said drive circuit has a level boosting circuit (P1, P2, N1, N3, N5, N6) with an output side connected to said input side of said blowing transistor.

10. The circuit configuration according to claim 1, wherein the circuit configuration is constructed using CMOS circuit technology.

11. A mass memory chip, comprising:

a circuit configuration, including:

a programmable link for permanent storage of a datum;

a drive circuit containing:

a data input;

a complementary data input;

a drive circuit output coupled to said programmable link and outputting an energy pulse for activating said programmable link in a manner dependent on a data signal present at said data input;

a first transistor having a control terminal connected to said data input;

a second transistor having a control terminal connected to said complementary data input; and

a volatile memory for storing a datum, said volatile memory containing:

an output outputting the data signal being a memory content of said volatile memory, said output connected to said data input of said drive circuit for data communication, said control terminal of said first transistor receiving the data signal; and

a complementary output outputting a complementary data signal being complementary to the data signal and connected to said complementary data input of said drive circuit, said control terminal of said second transistor receiving the complementary data signal.